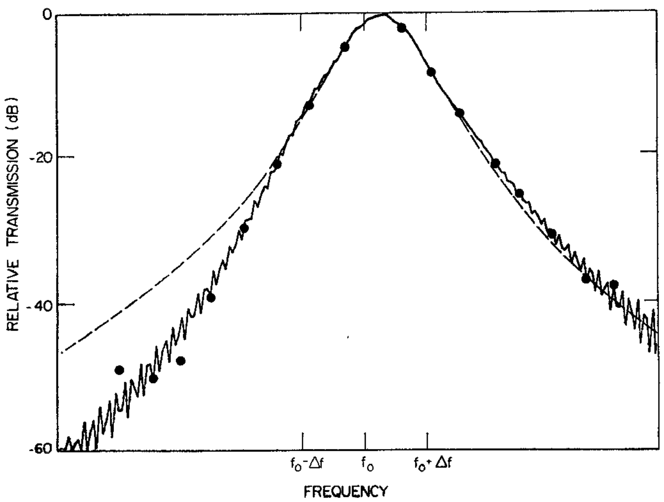

Fig. 2. Desired, theoretical, and experimental responses of bandpass filter.

that CW measurements were impractical, and long pulses at selected frequencies had to be used. The $LiNbO_3$ delay line had a center frequency of 30 MHz, a 3-dB bandwidth (Δf) of 5 MHz, and a finger grading which covers a frequency range of approximately 10–50 MHz. The unmatched insertion loss at the center frequency was 18 dB. The theoretical curve and the data show an asymmetry which is due to an improper compensation for the electrical mismatch of the graded finger spacing in the design (see [2]). This has been carried over to the theoretical curve to give an accurate comparison of theory with experiment.

This short paper has discussed a nonlinear FM technique for making SWDL bandpass filters. It has the advantage that very little or no apodization of the fingers is necessary, and thus diffraction losses of the delay line can be minimized. Further, it allows the designer the freedom to specify the time domain and frequency domain amplitude responses of a single transducer independent of one another. One disadvantage of these filters is that in practice their maximum center frequency is limited. This is because in an FM transducer the number of fingers required is determined by the center frequency and the time duration of the impulse response. Thus for applications with very high center frequencies, the number of fingers required may be more than can be practically fabricated. However, most applications occur in the range of 100 MHz or below where the number of fingers required is usually practical.

Acknowledgment

The author wishes to thank R. Price for helpful discussions.

References

[1] R. H. Tancrell and M. G. Holland, "Acoustic surface wave filters," *Proc. IEEE*, vol. 59, pp. 392–409, Mar. 1971.
[2] C. S. Hartmann, D. T. Bell, Jr., and R. C. Rosenfeld, "Impulse response design of surface acoustic wave filters," this issue, pp. 162–175.
[3] E. N. Fowle, "The design of FM pulse compression signals," *IEEE Trans. Inform. Theory*, vol. IT-10, pp. 61–67, Jan. 1964.

A Programmable Surface Acoustic Wave Matched Filter for Phase-Coded Spread Spectrum Waveforms

P. J. HAGON, F. B. MICHELETTI, R. N. SEYMOUR, AND C. Y. WRIGLEY

***Abstract*—A programmable surface acoustic wave (SAW) matched filter for biphase-coded spread spectrum waveforms has been constructed using a temperature-stable *ST*-cut quartz tapped delay line (TDL) and silicon-on-sapphire integrated control circuits. Construction is hybrid with wire stitch bond interconnections between the acoustic and microelectronic portions of the device. The SAW TDL operates at 120-MHz center frequency with 100-ns spacing between adjacent taps for a 10-MHz chip rate. The output of each tap can be individually switched to a load with 0 or 180° phase shift by the silicon-on-sapphire integrated control circuits. The high-speed capability of silicon-on-sapphire integrated circuits allows programming (code changing) to be achieved with a serial data input at 10-MHz rates, while the low temperature coefficient of *ST*-cut quartz allows satisfactory operation over a wide temperature range (−25°C to +85°C).**

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I. Introduction

Spread spectrum communication systems have been developed to provide efficient and reliable information transfer between source and receiver [1]. Waveform coding techniques are used to combat noise problems and to give security and multiple access capability [2]. Various waveform coding techniques are possible such as linear FM and phase-coded CW. Combinations of these waveforms in contiguous frequency channels and/or time-ordered sequences can be used. Whichever coding scheme is used, a necessary component in the receiver is the matched filter.

Surface acoustic wave (SAW) tapped delay line (TDL) matched filters for phase-coded waveforms have been developed with near-optimum performance and are now being incorporated in developmental spread spectrum communication systems. Current applications use fixed coded TDL's with center frequencies in the 30–200-MHz region with up to 511 taps for biphase-coded waveforms at 5–20-MHz chip rates. These basically passive devices have the advantages of low loss, small size, simplicity, and low cost when compared to previous TDL's utilizing bridged-T delay networks or electromagnetic cable delay lines. They are also significantly less complex than power-consuming digital processors which can perform similar functions.

To achieve the full potential of the TDL's and meet future system requirements, it will be necessary that individual taps of the TDL be programmable in order to process different codes [3]. It will also be highly desirable that the programming be accomplished in real time. That is, the TDL performing as a matched filter for an incoming phase-coded waveform must be switched rapidly enough to match another code without a time gap being required between the two received codes. This real-time programming capability will give security, immunity to multipath problems, and multiplexing capability. For many system applications additional requirements are low power drain and the ability to operate over a wide temperature range. For these reasons silicon-on-sapphire (SOS) technology has been used for the microelectronic control circuits and *ST*-cut quartz for the TDL.

SOS has a major advantage over other integrated circuit (IC) approaches in that parasitic capacitances are reduced to a minimum by virtue of the insulating sapphire substrate. High-speed IC's required for programmable tapped delay line (PTDL) applications can consequently be readily achieved. The piezoelectric acoustic medium (*ST*-cut quartz) was selected for its zero first-order temperature coefficient which allows device operation over the −25°C to +85°C temperature range with no significant variation in device performance.

The control microelectronics is described in Section II, and overall PTDL device performance is presented in Section III.

II. SOS Integrated Control Circuits

A modular approach was used in the control circuit design to ensure reasonable IC yields and to achieve flexibility which would allow extension to larger numbers of taps. An IC die[1] design was selected which provides control for 16 taps of a TDL. The functional block diagram of this die is shown in Fig. 1 and its operation is as follows.

A data register accepts serial digital information representing the desired tap switch positions and holds this data indefinitely by activation of the HOLD command. Parallel shifting of the data into the storage register is then accomplished by application of a transfer signal T. The storage register controls the switch drivers which set the tap switches according to the input data. At the end of the hold

[1] The "die" terminology is used to avoid confusion between the normally used IC "chip" of the semiconductor industry and the waveform "chip" of communication systems.

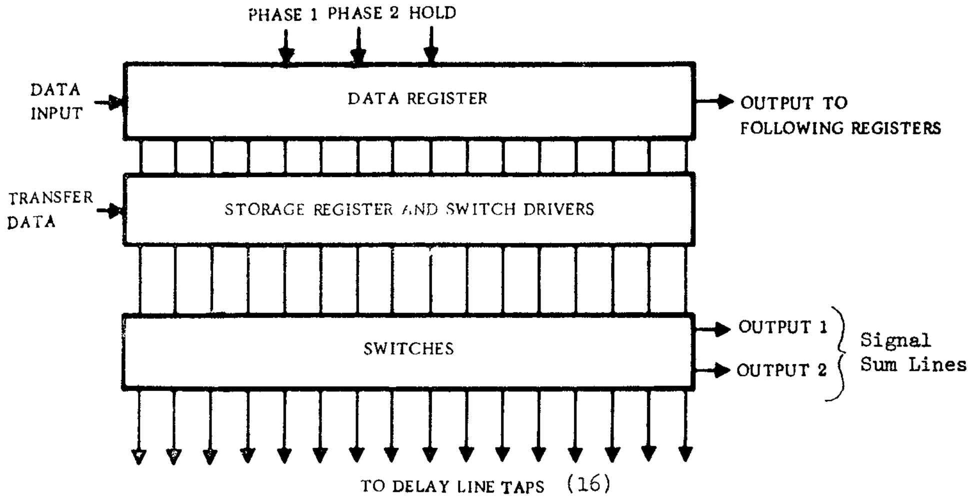


Fig. 1. Block diagram of SOS IC die for control of 16 taps.

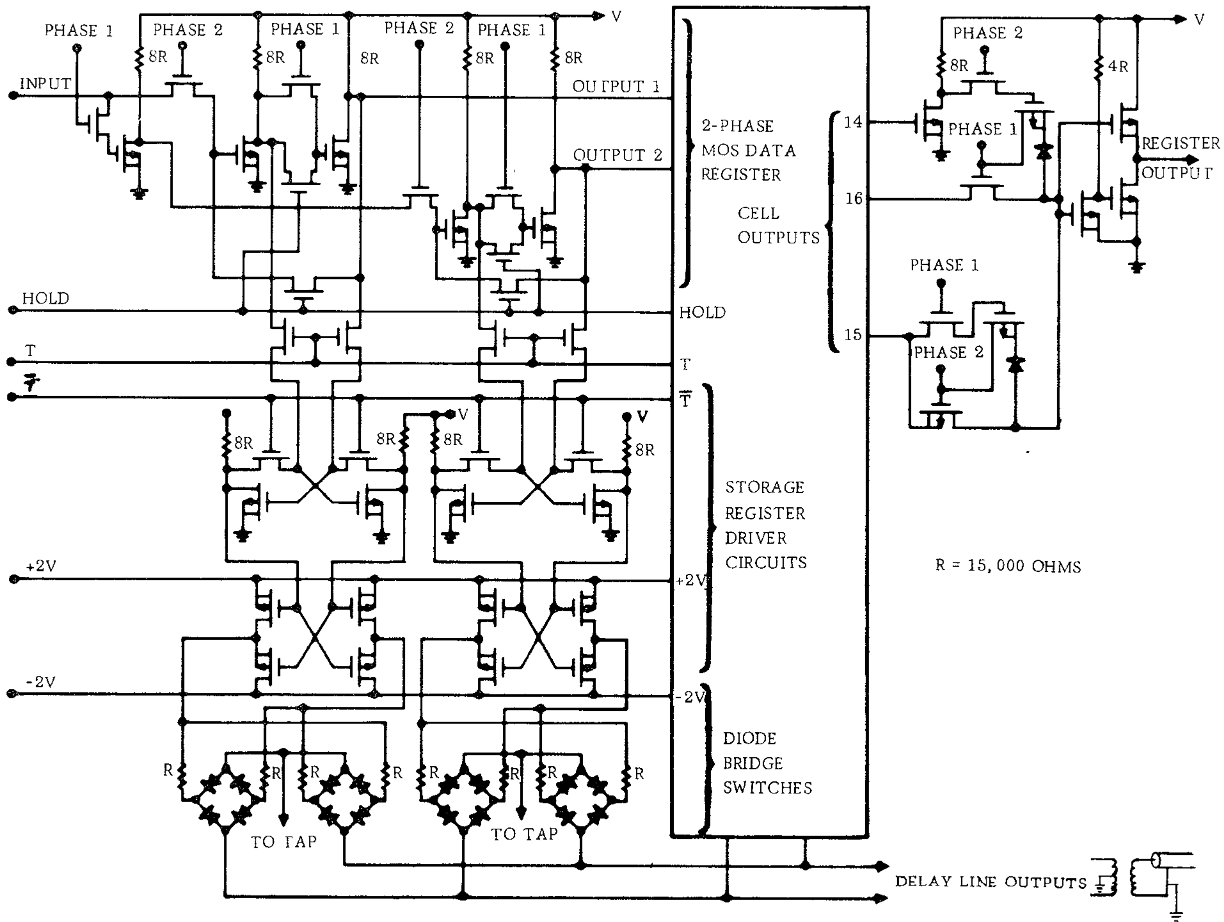


Fig. 2. SOS circuit for control of 16 taps.

and transfer period the data register is disconnected from the storage register and is free to accept new information. Meanwhile the taps are set to correlate with a particular incoming coded wave form. Provision is made in the circuit design to allow multiple IC chips to be connected in series to control 32, 48, 64, etc., taps. The actual circuit diagram of the control IC is shown in Fig. 2. The input data register is a dynamic two-phase clocked p-channel MOS shift register designed for 10-MHz input data rates with a static hold capability. The dual diode bridge implementation of the SOS diode switches is shown together with the storage register and driving circuits. Diode bridges are biased ON or OFF through 15-kΩ resistors from a ± 2-V supply. A 15-kΩ resistance is sufficient to provide isolation of the IF signal from the control circuit. Circuit design criteria are as follows:

digital input data rate	$\geq$10 MHz
data register	$\leq$4mW/stage
static storage register	$\leq$4mW/stage
drivers and diode bridges	$\leq$1mW/stage
IF frequency capability	$\leq$500 MHz
IC chip size	0.188 by 0.108 in.

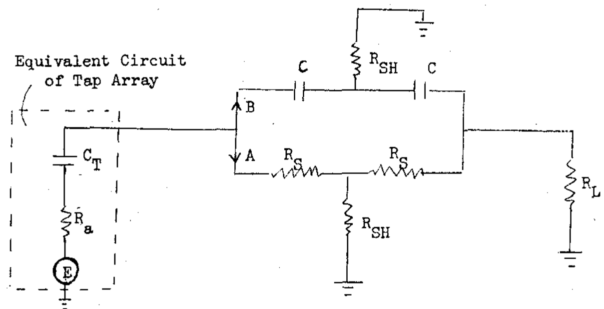


Fig. 3. Approximate net output circuit of PTPL.

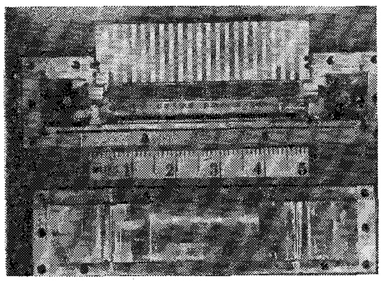


Fig. 4. PTDL.

The effect of diode bridge switch characteristics on TDL performance can be determined by reference to Fig. 3. This shows the equivalent circuit of the tap array connected to a load R_L (50 Ω) through 128 ON diode bridges (path A) and through 128 OFF diode bridges (path B). Series resistances (R_S) each represent the ON resistance of 248 diodes in parallel and are <1 Ω, while the shunt resistances R_{sh} represent 248 15-kΩ load resistors in parallel which equal 70 Ω. The latter represents an IF leakage path through the control circuit. Capacitances C each represent 248 reverse-biased diodes in parallel and are $\sim$4.9 pF (250-Ω reactance at 120 MHz). A simple analysis of this circuit design shows the increased insertion loss due to adding the switches over a fixed coded TDL is <3 dB, while the ratio of desired signal to the 180° out-of-phase signal through the OFF diode bridges (unwanted signal) is on the order of 20 dB.

The device processing sequence used to fabricate the SOS IC dice is very similar to that used for the MOS/LSI IC's that are in large scale production in the semiconductor industry.

The SOS approach eliminates the large parasitic capacitances between individual devices and a common conducting silicon substrate inherent in bulk silicon technology. Parasitic capacitances generally present low impedance shunts to ground and considerably reduce isolation resistance of OFF switches for analog signals. This can result in considerable signal loss that increases with frequency of operation.

III. Programmable Tapped Delay Line (PTDL)

A complete PTDL is shown in Fig. 4. It contains 1) a 128-tap ST-cut quartz delay line with 100-ns tap spacing that operates at 120-MHz center frequency, 2) 8 SOS control circuits each controlling 16 taps, 3) a toroidal inductor to tune the input IDT of the tapped delay line, 4) a center-tapped output transformer to combine the $+\pi/2$ and $-\pi/2$ signal lines into a single output, 5) a printed circuit connector card for introducing input data, clocks, hold and transfer signals, and bias voltages, 6) two omni spectra miniature (OSM) connectors for IF input and output. Package size excluding coaxial connectors is 3 by $\frac{3}{4}$ by $\frac{1}{2}$ in. The construction is hybrid with stitched aluminum wire bonds connecting control circuit chips with each other and with the SAW TDL, as shown in Fig. 5.

Fig. 6 shows a demonstrator box designed to exercise the PTDL. It contains a feedback shift register to generate p-n codes up to 2048 bit in length for data input in addition to clock generators and hold and transfer command generators. Two PTDL's can be accommodated in the box so that both autocorrelation and cross correlation can be demonstrated. In autocorrelation mode both PTDL's can be set to the same code, and a coded waveform generated by impulsing one PTDL can be fed into the other PTDL matched filter set to receive this code. The resultant autocorrelation function can be displayed on an oscilloscope. Different codes can also be set into the two PTDL's and the cross correlation of the two codes demonstrated.

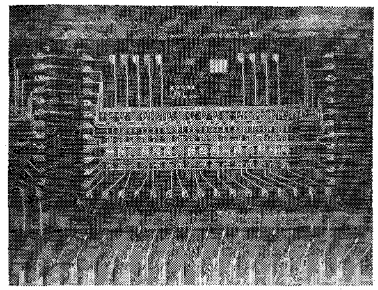


Fig. 5. SOS IC chip bonded in PTDL.

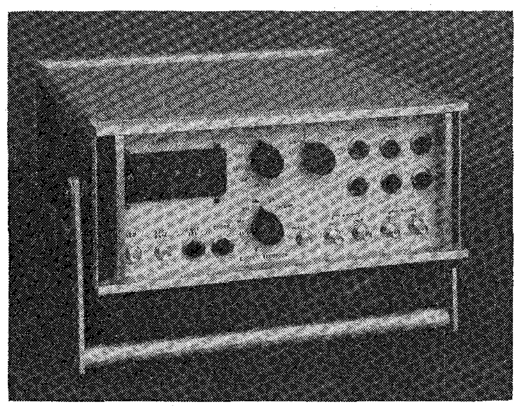
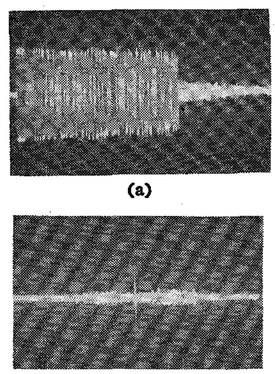


Fig. 6. PTDL exerciser.



(a)

(b)

Fig. 7. PTDL matched filter performance (input–output). (a) 127-chip biphase-coded waveform. Input to PTDL: 2 μs/div. (b) Output of PTDL: 5 μs/div.

Fig. 7(b) shows the autocorrelation function of a 127-chip p-n code obtained by feeding the expanded waveform of Fig. 7(a) into a PTDL set to correlate this code.

Insertion loss from input waveform to correlation peak is 27 dB compared with 22 dB obtained when a fixed coded TDL is used for the correlation. This means 5-dB insertion loss is added by the control and signal summing circuits compared to 3 dB expected from the design criteria. The correlation peak–highest sidelobe ratio in Fig. 7(b) is 20 dB, which represents good performance since tap apodization was not included in the acoustic TDL. Correlation peak width from null to null is the expected 200 ns.

Conclusions

Programmable surface acoustic wave tapped delay line matched filters for biphase-coded waveforms have been demonstrated using an approach that should result in performance levels within 3 dB of fixed coded SAW TDL performance. The SOS IC approach to programming and control functions used for this demonstration offers an excellent combination of high-speed and low-power capability that are important requirements of future communication systems. Extension of this approach to matched filters capable of real-time programming at 50-MHz rates with several hundred taps is considered feasible.

References

[1] M. G. Unkauf, "Spread spectrum communications and modems," presented at the IEEE Ultrasonics Symp., Miami Beach, Fla., Dec. 1971, Paper M-1.

[2] D. T. Bell, Jr., J. D. Holmes, and R. V. Ridings, "Application of acoustic surface wave technology to spread spectrum communications," this issue, 263–271.

[3] E. J. Staples and L. T. Claiborne, "A review of device technology for programmable surface wave filters," this issue, pp. 279–287.

Generation of Pseudonoise Sequences Using Surface Acoustic Waves

D. P. MORGAN AND J. G. SUTHERLAND

***Abstract*—Pseudonoise sequences can be generated by using a surface acoustic wave delay line in place of a shift register. Modulo-2 addition is achieved by combining the outputs of two transducers and using envelope detection. A 31-bit pseudonoise sequence was generated with a bit period of 1.1 μs.**

Pseudonoise sequences are conventionally generated by using shift registers with logical feedback [1]. The logic function can be a modulo-2 addition of the states of two or more stages and is illustrated in Fig. 1(a) for two stages. Appropriate logic functions have been given [2] for a wide variety of sequences. In this short paper we describe a method in which the shift register is replaced by a surface acoustic wave delay line. This technique is in principle capable of producing higher bit rates than are currently available by purely microelectronic means, although the bit rate for one device will not be variable over a wide range.

A modulo-2 adder gives a logical "1" output when the two inputs are different and a logical "0" when the inputs are the same. This can be done in a variety of ways using surface acoustic waves, one method being shown in Fig. 1(b). Here a surface-wave delay line has three interdigital transducers, and a logical "1" input is represented by an RF pulse while a logical "0" input is represented by the absence of a pulse. The two output transducers, which are connected together, are arranged such that they give RF otuput voltages which are 180° different in phase, giving cancellation when they are both excited. This arrangement is a modulo-2 adder if the presence of RF at the output, irrespective of its phase, is taken as a logical "1."

The device was constructed to generate a 31-bit pseudonoise sequence by modulo-2 addition of the third and fifth stages. Ideally this requires the two output transducers to be situated at distances $3T/V$ and $5T/V$ from the input transducer, where T is the length of 1 bit in the sequence and V is the surface-wave velocity. In practice, the threshold circuit is set to reject spurious pulses, and this involves a small delay which is compensated by a timing advance A in the position of the input transducer. This arrangement also serves to prevent small timing errors from becoming cumulative. The delay line output is detected and used to trigger a monostable which produces pulses of length less than T. The mixer gates a carrier to give RF pulses which are fed to the delay line input.

The delay line was constructed on a lithium niobate substrate, with a center frequency of 35 MHz and with $T = 1.1$ μs. Fig. 2 shows the waveforms produced, where the repetition period is $31T$. The system can quite readily be synchronized to an external clock, and this would allow the bit rate to be varied over a small range.

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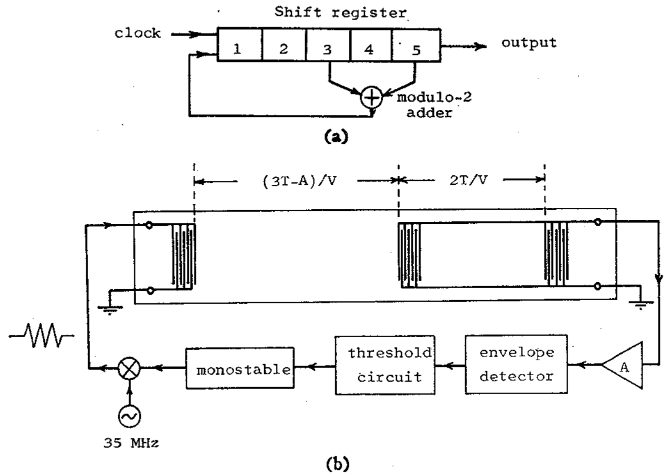

Fig. 1. (a) 5-stage shift register used to generate 31-bit pseudonoise sequence. (b) Arrangement for generation of the same sequence using surface acoustic wave delay line.

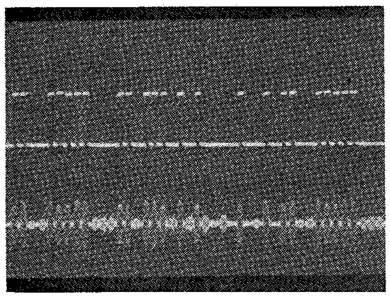

Fig. 2. Upper trace: Output of monostable. Lower trace: Output of delay line. Horizontal scale: 5 μs/div. Waveforms correspond to 31-bit pseudonoise sequence 1111100011011101010000100101100.

It is envisaged that surface-wave pseudonoise generators offer significant advantages over conventional methods when high bit rates are required, for example, in testing wide-band microwave communication links. At high bit rates microelectronic pseudonoise generators are limited by delay in the feedback circuit and difficulty of obtaining exactly synchronous clocking of all elements in the system. This limits the bit rate obtainable to about half the logic rate capability of the circuitry, i.e., to about 150 Mbit/s using MECL-III. In contrast, the surface-wave approach does not require synchronous clocking, and feedback delay can be compensated by appropriately positioning the transducers, so that in principle the bit rate can be as high as the circuitry logic rate, or 300 Mbit/s using MECL-III. Bandwidths of this order can be obtained using surface waves, and van de Vaart and Schissler [3] have demonstrated a digital delay line using surface waves at 220 Mbit/s. In addition, the surface-wave delay line is passive, and for storage of larger numbers of bits at high bit rates it has a significant cost advantage as compared to a microelectronic shift register.

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References

[1] M. P. Ristenbatt, "Pseudo-random binary coded waveforms," in *Modern Radar*, R. S. Berkowitz, Ed. New York: Wiley, 1965.

[2] W. W. Peterson, *Error-Correcting Codes*. Cambridge, Mass.: M.I.T. Press, 1961.

[3] H. van de Vaart and L. R. Schissler, "Acoustic-surface-wave recirculating memory," *Electron. Lett.*, vol. 8, pp. 333–334 ,1972.